Design and Characterization of Ionizing Radiation-Tolerant CMOS APS Image Sensors up to 30 Mrd (Si) Total Dose

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***Abstract*—An ionizing radiation-tolerant CMOS active pixel sensor (APS) image sensor test chip was designed employing the physical design techniques of enclosed geometry and P-channel guard rings. The test chip was fabricated in a standard 0.35-μm CMOS process that has a gate-oxide thickness of 7.0 nm. It was irradiated by a γ-ray source up to a total ionizing radiation dose level of approximately 30 Mrd (Si) and was still functional. The most pronounced effect was the increase of dark current, which was linear with total dose level. The rate of dark current increase was about 1 to 2 pA/cm^2/Krd (Si), depending on the design of the pixel. The results demonstrate that CMOS APS image sensors can be designed to be ionizing radiation tolerant to total dose levels up to 30 Mrd (Si). The fabrication process is standard CMOS, yielding a significant cost advantage over specialized radiation hard processes.**

***Index Terms*—Active pixel sensor, CMOS active pixel sensor, CMOS APS, dark current, image sensor, imager, ionizing radiation, ionizing radiation-induced dark current, ionizing radiation-tolerant CMOS APS, radiation hard, radiation tolerant.**

I. Introduction

CMOS active pixel sensor (APS) image sensors are fabricated in standard CMOS processes, the same processes that have been employed over the years in fabricating many digital and analog integrated circuits. On the other hand, charge-coupled device (CCD) image sensors, the incumbent image sensing technology, require specialized fabrication processes. Consequently, CMOS APS image sensing technology may enjoy three advantages over CCD image sensing technology.

The first advantage is that by employing the same CMOS fabrication process, CMOS APS image sensing arrays can be monolithically integrated with other CMOS digital and analog circuits such as timing-and-control modules, analog signal-processing circuits for noise suppression, analog-to-digital converters, and other application-specific analog and digital circuits. The exploitation of this advantage leads to a highly integrated, highly functional, and highly compact imaging system, commonly referred to as a camera-on-a-chip. The body of published work in this area is rather extensive. Some examples are described in [1]–[13].

The second advantage is that CMOS APS image sensors can be designed to be low power, utilizing the same design techniques that have been developed over the years for low-power CMOS digital and analog circuits. An example that illustrates this low-power feature is the CMOS APS image sensor described in [13] and [14]. At video rate, 30 frames per second (fps), that image sensor consumes about 550 μW at a 1.5-V power supply. A camera based on that image sensor can operate on a single watch battery for a long time.

The third advantage is economic. Compared to the volume of CCD-based integrated circuits, the volume of CMOS integrated circuits fabricated each year is very high because it encompasses not only image sensors but also many other CMOS digital and analog integrated circuits, including microprocessors. Hence the cost of a CMOS-based imaging system should be less than its CCD-based counterpart.

Because of the three features described above, CMOS APS technology is emerging as a viable alternative to CCD technology for power, mass, and cost constrained imaging systems. A primary set of such applications is space-based applications. A CMOS APS image sensor has already been developed for star and feature tracking applications [15], [16]. A star tracker guides and controls the spacecraft by observing, identifying, and tracking star fields. However, the CMOS APS image sensor has to be tolerant to radiation in order to be space qualified. Consequently, it is essential for the applications of image sensor-based spacecraft instrumentation that CMOS APS image sensors are designed and fabricated to be radiation tolerant. Furthermore, fabricating the radiation-tolerant CMOS APS image sensors in standard CMOS processes provides a considerable cost advantage over other image sensors fabricated in specialized radiation-tolerant processes.

Image sensors are inherently susceptible to pixel leakage current, which accumulates a charge signal even in the absence of photons (dark current). Controlling dark current, in terms of both background level and uniformity across the array, is fundamental for a standard CMOS foundry to viably fabricate image sensors. Employment of physical design techniques to control a potential source of dark current has become necessary. Modifications to the CMOS fabrication process to better control dark current are sometimes required as well.

The three major and consequential effects of ionizing radiation on standard CMOS devices are shift of threshold voltages,

Manuscript received July 17, 2001. This work was supported in part by the NASA Goddard Space Flight Center under a SBIR Phase II award.

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Publisher Item Identifier S 0018-9499(01)10529-0.

leakage current in NMOS transistors, and N-channel intertransistor (isolation field) leakage current. The physical design technique of enclosed geometry proved to be very effective for significantly reducing leakage current in NMOS transistors [17], [18]. The N-channel intertransistor (isolation field) leakage current was substantially curtailed, employing the physical design technique of P-channel guard rings [17], [18]. Employing design techniques to enhance the radiation tolerance of integrated circuits, hardness-by-design [19] is gaining more acceptance because of the strong economic case that it presents.

The magnitude of ionizing radiation-induced threshold voltage shift is proportional to the number of holes created (and trapped) in the gate oxide due to ionizing radiation, which is proportional to its thickness (volume). Therefore, the magnitude of ionizing radiation-induced threshold voltage shift is smaller for thinner gate oxides. For particularly thin oxides (less than 12 nm thick), the ionizing radiation-induced holes in the gate oxide have a much better chance to tunnel out of the oxide (requiring only 6 nm effective tunneling distance) than to diffuse to the silicon/silicon dioxide interface. Ionizing radiation-induced threshold voltage shifts for both N- and P-channel transistors were experimentally found to get considerably smaller when the gate oxide is less than 12 nm thick [20], a feature of standard deep submicrometer CMOS technologies such as 0.35-μm technology.

An awareness of the significance of radiation-tolerant CMOS APS image sensors is emerging. This emerging awareness manifests itself by the recent publication of research work in this area [21]–[28]. However, none of the approaches described in these publications combines the employment of the physical design techniques of enclosed geometry and P-channel guard rings and a standard deep submicrometer CMOS fabrication process (having a thin gate oxide), resulting in image sensors that are tolerant to total ionizing radiation dose levels up to 30 Mrad (Si). In [21], a 512×512 photodiode (PD) CMOS APS image sensor, with a pixel size of 25×25 μm^2, is reported. The process used to fabricate the image sensor was a standard 0.7-μm process. The image sensor was γ-ray irradiated up to a total dose level of 21 Krd (Si). A large increase in dark current was reported above 6 Krd (Si). At 21 Krd (Si), the mean dark current density was about 45 nA/cm^2. It was reported that this dark current was large enough to saturate the image sensor at 0.75-MHz pixel rate at room temperature. No data were reported beyond 21 Krd (Si). In [22] and [25], a 32×32 PD CMOS APS and a 32×32 photogate (PG) CMOS APS image sensors, with a pixel size of 50×50 μm^2, are reported. The process used to fabricate the image sensors was a standard 1.2-μm process. The image sensors were γ-ray irradiated up to a total dose level of 10 Krd (Si). At 10 Krd (Si), the PD image sensor dark current was about 1.5 nA/cm^2, while the PG image sensor dark current was about 25 nA/cm^2. It was reported that the mean dark current increase did not vary linearly with dose level. No data were reported beyond 10 Krd (Si). In [28], a 32×32 PD CMOS APS image sensor, with a pixel size of 26.4×26.4 μm^2, is reported. The process used to fabricate the image sensor was a standard 1.2-μm process. The image sensor was irradiated up to a total dose level of 10 Krd (Si). At 10 Krd (Si), the dark current was about 6 nA/cm^2. It was reported that the dark current increased dramatically with radiation. No data were reported beyond 10 Krd (Si). In [27], it was observed that CMOS image sensors fabricated in standard processes exhibited an anomalous rise in dark current with radiation, the dark current rose exponentially with total ionizing dose, and the devices were failing to operate after having been irradiated beyond 50 Krd (Si). The measured dark current after 50 Krd (Si) of total dose was greater than 5 μA/cm^2. A γ-ray irradiation experiment was performed on an image sensor that was fabricated in a standard 0.5-μm process, with a pixel size of 12×12 μm^2. The image sensor was cooled to 220 K and was held at that temperature during the experiment, in which it was irradiated up to 25 Krd (Si) total dose. The dark current was observed to be well behaved and small, rising linearly with dose. However, after 25 Krd (Si) total dose, the image sensor went through a catastrophic and permanent failure, with radiation-induced dark current large enough to saturate the pixels. Annealing made no difference.

In [23], [24], and [26], PD CMOS image sensors and some test structures fabricated in standard 0.5-μm and 0.7-μm processes are reported. The image sensor format is 512×512 and the pixel size is 25×25 μm^2. Dark signal data for two image sensors that were fabricated in the 0.7-μm process were reported. The first image sensor pixel has a PMOS PD, while the second image sensor pixel has an NMOS PD. The PMOS image sensors were γ-ray irradiated up to a total dose level of 3.4 Mrd (Si). The dark signal was about 1.25 V/s. Neither the PD capacitance nor the conversion gain for this pixel was reported, so dark current density cannot be estimated. The NMOS image sensor was also irradiated up to 3.4 Mrd (Si). Then, it was left to anneal at room temperature for 562 h. After annealing, the irradiation was resumed to a total dose level of 22.5 Mrd (Si). The dark signal was about 0.8 V/s. At the reported PD capacitance (10 fF), the dark current density is estimated to be about 7 nA/cm^2. The dark current increase was rather linear, at an estimated rate of about 3.5 pA/cm^2/Krd (Si). This result is better than the results of other previous work (as described above). However, it includes the 562-h room-temperature annealing effect. No dark current data without the anneal effect was reported. The pixel design was not reported as well. In [27], a 256×256 CMOS image sensor, with a pixel size of 20×20 μm^2, is reported. The image sensor is fabricated in a specialized radiation hard 0.5-μm process. Some physical design techniques, such as surround-gate pixel, were employed in the design of the image sensor. The measured preradiation dark current was about 30 nA/cm^2. The image sensor was γ-ray irradiated up to a total dose level of 5.5 Mrd (Si). The increase in dark current was rather linear, at a rate of about 6 pA/cm^2/Krd (Si). This result is comparable to that obtained in [23], [24], and [26]. However, the high preradiation dark current (30 nA/cm^2) represents a major obstacle to deploying this image sensor in an imaging system. Furthermore, this image sensor was fabricated in a specialized radiation hard process, which is usually more costly (by at least a factor of two) than standard processes. Table I outlines the features and the dark current data reported for each of the image sensors of the previous work described above.

We have hypothesized that employing the physical design techniques of enclosed geometry and P-channel guard rings in a standard submicrometer CMOS technology that has a

TABLE I
COMPARISON OF PREVIOUS WORK ON TOLERANCE OF CMOS APS IMAGE SENSORS TO IONIZING RADIATION

Reference and Year	Array Size	Pixel Size	Fabrication Process	Maximum Total Dose (Si)	Dark Current at Maximum Total Dose	Comments
[21] 2000	512 X 512	25 μm X 25 μm	0.7 μm Standard	21 Krd	45 nA/cm^2	PD
[22], [25] 2000 and 1999	32 X 32	50 μm X 50 μm	1.2 μm Standard	10 Krd	1.5 nA/cm^2 25 nA/cm^2	PD PG
[28] 1997	32 X 32	26.4 μm X 26.4 μm	1.2 μm Standard	10 Krd	6 nA/cm^2	PD
[27] 2001	Not reported	12 μm X 12 μm	0.5 μm Standard	25 Krd [a]	Not reported [b]	220° K
[23], [24], [26] 2000 and 2001	512 X 512	25 μm X 25 μm	0.5 μm and 0.7 μm Standard [c]	3.4 Mrd 22.5 Mrd	1.25 V/s 0.8 V/s	PMOS PD NMOS PD [d,e]
[27] 2001	256 X 256	20 μm X 20 μm	0.5 μm Specialized	5.5 Mrd	60 nA/cm^2	PD [f]

a) After 25 Krd (Si), the image sensor went through a catastrophic and permanent failure.
b) Dark current was reported to be large enough to saturate the pixels (no pixel rate or frame rate was reported).
c) Some test structures were fabricated in the 0.5-μm standard process, but the reported dark current data was for image sensors fabricated in the 0.7-μm standard process.
d) Irradiation of the NMOS PD pixel chip was stopped after 3.4 Mrd. The chip was left to anneal at room temperature for 562 hours before irradiation resumed.
e) Neither conversion gain nor PD capacitance was reported for the PMOS PD pixel. Based on the PD capacitance reported for the NMOS PD pixel (10 fF), its dark current is about 7 nA/cm^2.
f) Pre-radiation dark current was 30 nA/cm^2.

gate-oxide thickness of 12 nm or less will significantly enhance the ionizing radiation tolerance of CMOS APS image sensors. A CMOS APS image sensor test chip was designed using the above-described physical design techniques. The process used to fabricate the test chip is a standard 0.35-μm CMOS process, with a gate-oxide thickness of approximately 7.0 nm. The test chip was then γ-ray irradiated to total ionizing radiation dose levels up to 30 Mrd (Si) and characterized.

In this paper, the design and characterization of the test chip are presented. This paper has four main sections. Section II describes the test chip. Section III presents the irradiation experiment setup and results. Section IV describes the ionizing radiation induced dark current and its mechanism. Section V is a discussion, followed by conclusions in Section VI.

II. DESCRIPTION OF TEST CHIP

The physical design techniques of enclosed geometry and P-channel guard rings were used to design and lay out a set of four N-type radiation tolerant active PD pixels. The four pixels have the same circuit schematic diagram, which is shown in Fig. 1. As revealed by the circuit schematic diagram, each pixel can be reset individually independent of its row or its column within the pixel array. The feature of individual pixel reset is important for some space applications such as star and feature tracking. The layout of the four pixels (Pixel0, Pixel1, Pixel2, and Pixel3) is shown in Fig. 2. The size of each of the pixels is 16.2×16.2 μm^2. To enhance the photosensitivity, the photodiode area of each of the four pixels is designed not to have the salicide layer. The salicide layer has the advantage of lowering the resistance (for example, p-n junction series resistance or polysilicon sheet resistance) but has the drawback of transmitting less of the incident photons through to the silicon underneath. The drawn area of the photodiode of Pixel0 is 61.2 μm^2 and the drawn length of its perimeter is 34.8 μm. The drawn area

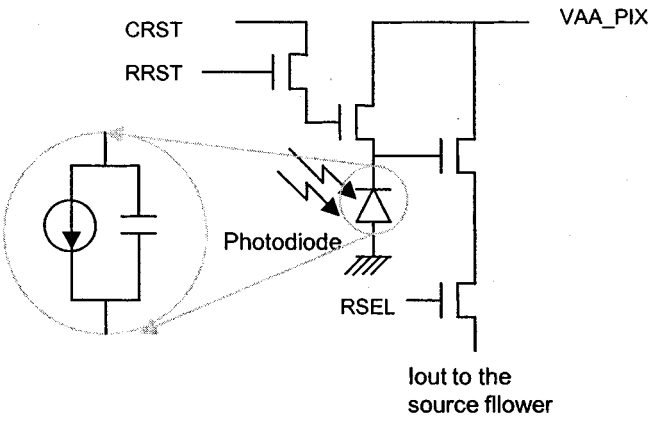

Fig. 1. The circuit schematic diagram of the pixel used in the test chip.

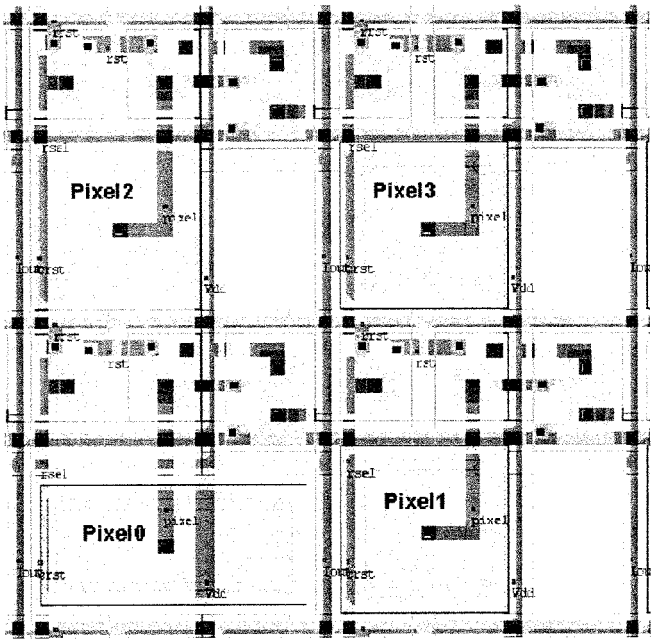

Fig. 2. The layout of the four different pixels used in the test chip.

of each of the photodiodes of Pixel1 and Pixel3 is 15.9 μm^2 and the drawn length of the perimeter is 14.1 μm. The drawn area of the photodiode of Pixel2 is 64.0 μm^2 and the drawn length of its perimeter is 32.0 μm. Each of the photodiodes of Pixel1 and Pixel3 is designed to have an N-well to further enhance the photosensitivity. Each of the metal contacts to the photodiodes of Pixel1 and Pixel2 is designed not to have the salicide layer, while each of those of Pixel0 and Pixel3 is designed to have the salicide layer. This was done to assess the impact of the salicide layer on various performance parameters, particularly photosensitivity and levels of pre- and postradiation dark current. Table II summarizes the key design parameters for each of the four pixels.

The four pixels were compiled into a pixel array. The array size is 256×256, constituting an imaging area of approximately 4.1×4.1 mm^2. The array was divided into four subarrays, each 128×128. Each of the four subarrays has only one of the four pixels. The peripheral circuits were then integrated around the pixel array. The peripheral circuits were designed to be ionizing radiation tolerant, employing the same design techniques

TABLE II
KEY DESIGN PARAMETERS FOR EACH OF THE FOUR PIXELS

Design Parameter	Pixel0	Pixel1	Pixel2	Pixel3
PD drawn area (μm^2)	61.2	15.9	64.0	15.9
PD drawn perimeter (μm)	34.8	14.1	32.0	14.1
N-well PD	No	Yes	No	Yes
Salicide layer of the PD area.	No	No	No	No
Salicide layer of the PD metal contact	Yes	No	No	Yes
Recessed n^+ implant	Yes	Yes	No	Yes
Drawn fill factor (ratio of PD area to total pixel area)	23.3%	6.1%	24.4%	6.1%

TABLE III
PRIMARY PARAMETERS OF THE FABRICATION PROCESS

Fabrication process parameter	Description
Technology	0.35-μm Standard CMOS
Process	Mixed mode, twin well
Supply voltage	3.3 V
Gate oxide thickness	7.0 nm
Device isolation	LOCOS
Number of polysilicon layers	1 or 2 (2 were used)
Number of metal layers	2 to 5 (3 were used)

used in the pixel array. The main peripheral circuits are row and column decoders, row buffers, and an analog circuit processor. The row and column decoders are similar and are used to select the particular row(s) and column(s) of the array that are under consideration at a given time. The windowing function and the electronic pan and tilt functions can be realized by manipulating the digital inputs of those decoders. The row buffers are used to drive the pixel control signals, such as reset and row select, to the pixels across the array. The analog signal processor is used to sample-and-hold the output signal voltage level (illuminated level) and the output voltage reset level (dark level). Pseudocorrelated double sampling (Pseudo CDS) is realized off-chip by taking the difference between those two analog voltage levels. This difference constitutes the analog output video signal.

The chip was fabricated employing a standard 0.35-μm CMOS fabrication process. Table III shows the primary parameters of the fabrication process. The total size of the die is approximately 5.2×5.0 mm^2. The total number of the I/O pads on the test chip is 42. A 121-pin ceramic pin grid array (PGA) package was used to house the die. A photograph of the die attached to the package and wire bonded is shown in Fig. 3. Table IV shows the main features of the test chip.

III. IRRADIATION EXPERIMENT SETUP AND RESULTS

The irradiation of the test chip was performed using a Co^{60} γ-ray radiation source. The MIL-STD-883E, Method 1019.5, Ionizing Radiation (Total Dose) test standard was followed. The software and hardware of the camera board system were modified for more automated image data acquisition. The captured images were saved as raw data during measurement. Another piece of software was used to analyze the data. Irradiation and measurements were performed at ambient temperature and pressure. Output video signal was measured under both dark and illumination conditions and at multiple total dose levels ranging from 50 Krd (Si) up to 30 Mrd (Si). The intermediate total dose levels at which measurements were performed are approximately 100, 200, 300, and 500 Krd (Si) and 1, 2, 5, 10, and 20 Mrd (Si). During irradiation, the image sensor test chip was biased and pixels were set to reset voltage level, simulating actual operation. At all the total dose levels, up to and including approximately 30 Mrd (Si), the image sensor test chip was functional. The highest total dose level to which the image sensor test chip was exposed (approximately 30 Mrd (Si)) was the highest total dose level that can be realized within the time allocated to the irradiation experiment.

The output video signal voltage under dark conditions was measured for each pixel within the pixel array by integrating the test chip image sensor in the dark for a certain integration

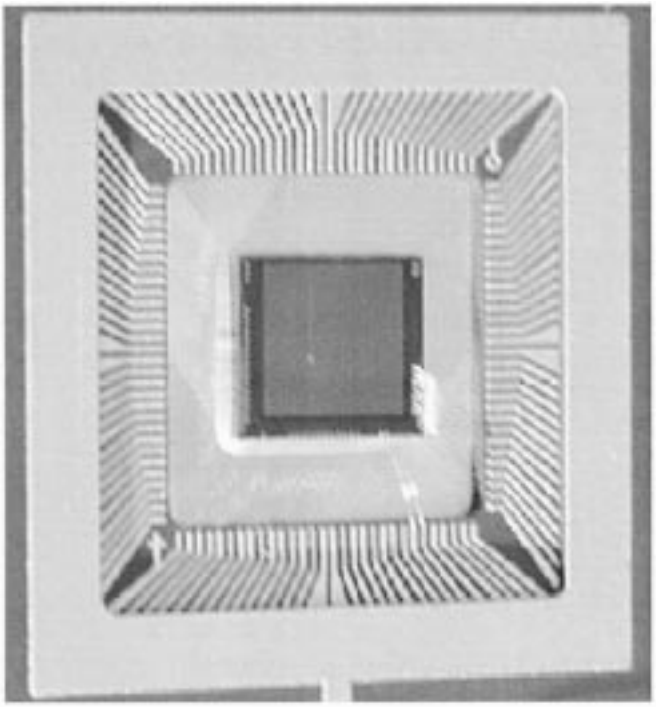

Fig. 3. A photograph of the die in its package.

TABLE IV
MAIN FEATURES OF THE TEST CHIP

Feature	Description
Pixel array size	256 X 256
Pixel size	16.2 μm X 16.2 μm
Imaging area	4.1 mm X 4.1 mm
Number of pixel sub-arrays	4
Pixel sub-array size	128 X 128
Output	Analog
Individual pixel reset (regional shutter)	Yes
Electronic windowing, panning, and tilting	Yes
Die size	5.2 mm X 5.0 mm
Number of I/O pads	42
Package	121-pin ceramic PGA

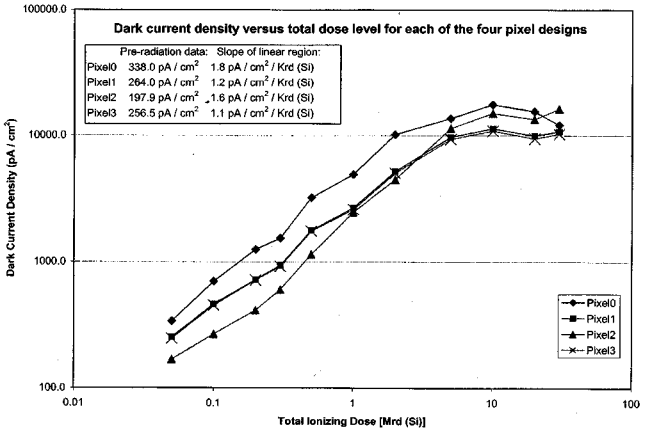

Fig. 4. Dark current density versus total dose level for each of the four pixels.

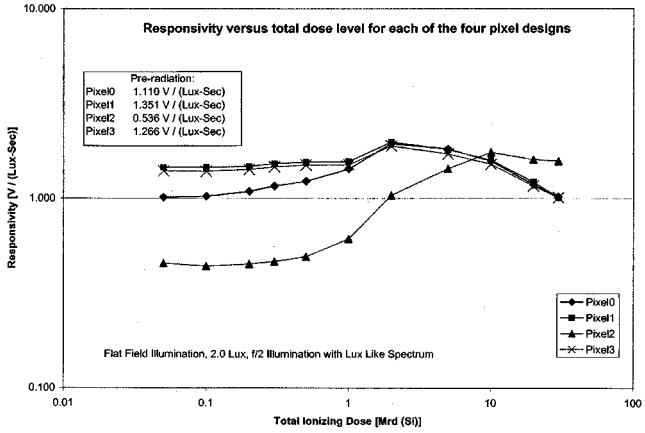

Fig. 5. Responsivity versus total dose level for each of the four pixels.

TABLE V
CONVERSION GAIN, SATURATION VOLTAGE, AND PIXEL ELECTRON CAPACITY FOR EACH OF THE FOUR PIXELS

Pixel	Conversion gain (μV/e)	Saturation voltage (V)	Pixel electron capacity (Ke)
Pixel0	9.88	0.74	74.9
Pixel1	13.30	0.59	44.4
Pixel2	9.80	0.90	91.9
Pixel3	13.30	0.57	42.9

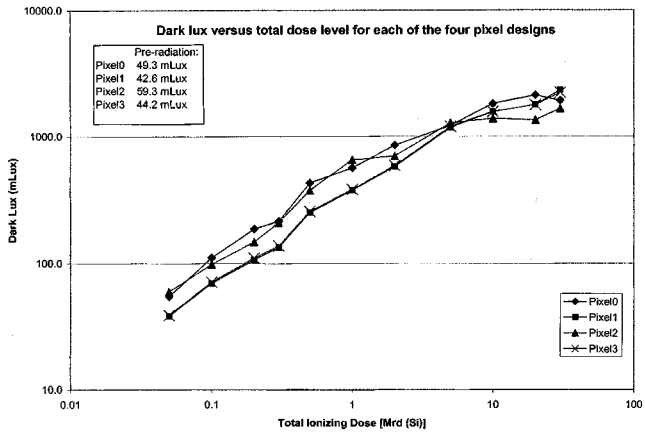

Fig. 6. Dark lux versus total dose level for each of the four pixels.

time. The average dark output voltage of a specific pixel type was calculated by averaging the dark output voltages from all the relevant pixels within that pixel-type subarray. Then, the integration time was varied (six values of integration time were used) and the corresponding average dark output voltages were measured for each pixel type (16 frames of data were acquired at each integration time). The average dark output voltage was then plotted against integration time (for each pixel type), producing a straight line, the slope of which is the average dark signal (dark output voltage per unit time). Then, the conversion gain and the area of each pixel were factored in, and the average dark current per unit area was obtained. The data are presented in Fig. 4, which shows the average dark current density in pA/cm^2 versus the total dose level in Mrd (Si) for each of the four pixels. It should be noted that the conversion gain of each pixel is dependent on its design and on the fabrication process. The conversion gain for each of the pixels was calculated based on the experimental results of comparable test structures. The test structures were designed to measure the area capacitance and the perimeter capacitance of the relevant photodiodes. Table V shows the conversion gain, measured saturation voltage, and resultant pixel electron capacity (number of electrons needed to reach saturation) for each of the four pixels.

In a similar manner of measuring the output video signal voltage under dark conditions, the output video signal voltage under illumination was measured. The light source used has a lux-like spectrum, simulating the response of the human eye. The light source projected a flat field of illumination on the surface of the image sensor test chip. The current controlling the output light brightness level of the light source was adjusted such that the light brightness level measured at the surface of the test chip was approximately 2.0 lux. The aperture of the light source and its distance to the test chip were such that the equivalent f-number of the optical system was 2.0. The integration time was varied and the corresponding average output voltages were measured for each pixel type. The average output voltage was then plotted against exposure (which is defined as the multiplication of the light brightness level by integration time), producing a straight line, the slope of which is the average responsivity (output voltage per unit light brightness level per unit time). The data are presented in Fig. 5, which shows the average responsivity in V/(lux.s) versus the total dose level in Mrd (Si) for each of the four pixels.

It is most desirable to have an image sensor with both high responsivity and low dark signal. To be able to assess both performance parameters concurrently, the concept of *dark lux* is used. The dark lux of an image sensor is a figure of merit that combines both the responsivity and the dark signal of the image sensor. It is obtained by dividing the dark signal (V/s) by the responsivity [V/(lux.s)]. The dark lux reveals how much equivalent light the image sensor requires to output a voltage signal equal to its dark signal, independent of integration time. The lower the dark lux is for an image sensor, the better its combined dark signal and responsivity performance is. The dark lux (in mlux) versus the total dose level [in Mrd (Si)] is shown in Fig. 6 for each of the four pixels.

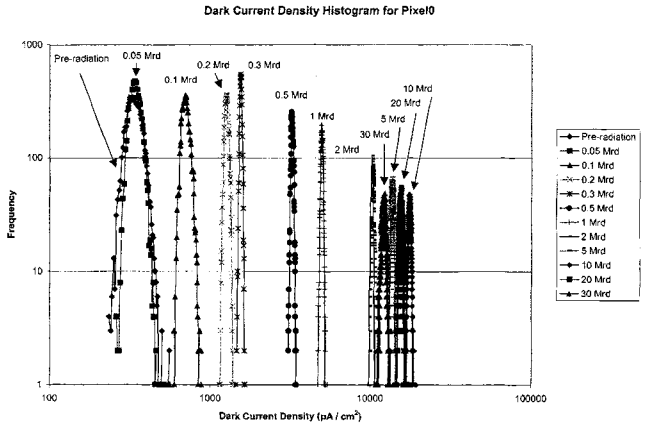

Fig. 7. Dark current density histograms for Pixel0.

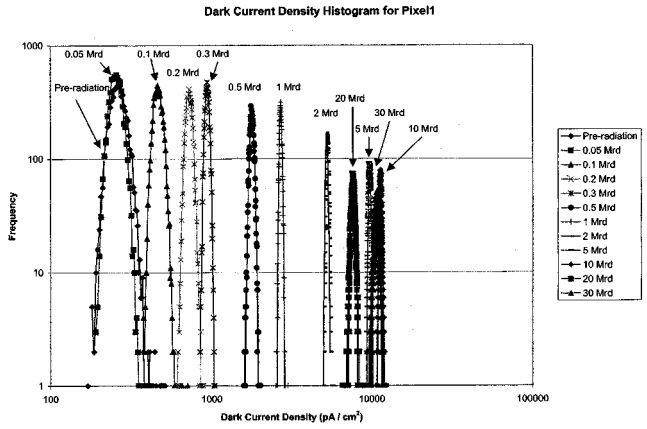

Fig. 8. Dark current density histograms for Pixel1.

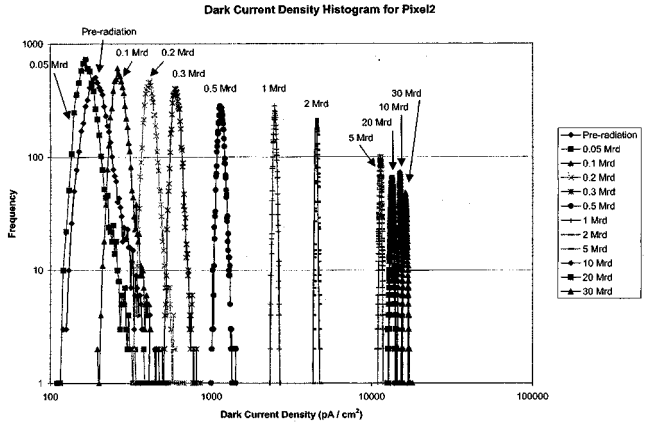

Fig. 9. Dark current density histograms for Pixel2.

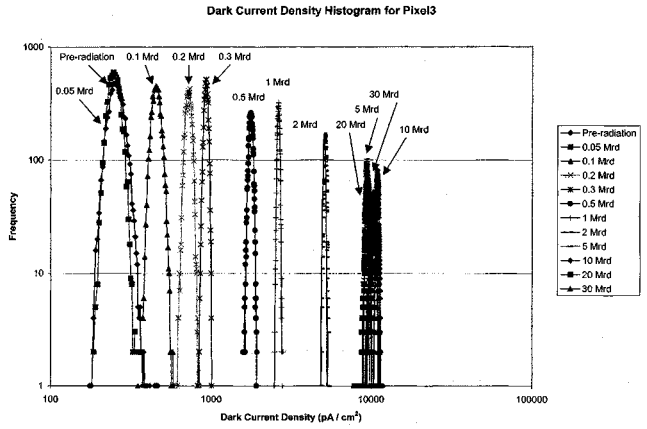

Fig. 10. Dark current density histograms for Pixel3.

The dark current density data presented in Fig. 4 is an average dark current density data. It was obtained for a specific pixel type by averaging the dark output voltages from all the relevant pixels within that pixel type subarray. While the data presented in Fig. 4 are very useful for assessing the impact of ionizing radiation on dark current, they have the disadvantage of concealing dark current nonuniformity across the pixel type subarray. To assess the dark current nonuniformity, a dark current density histogram approach was utilized. In this approach, the count (frequency) of relevant pixels, within the specific pixel-type subarray, having the same dark current density is plotted against the dark current density. This histogram plot was done for each total ionizing radiation dose level. The resultant set of histograms for Pixel0 is depicted in Fig. 7. Similar sets of histograms are depicted in Figs. 8–10 for Pixel1–Pixel3, respectively.

IV. Ionizing Radiation-Induced Dark Current

A simplified cross-section of a typical PD-type CMOS APS pixel is schematically illustrated in Fig. 11. The primary part of this pixel is the PD, which may be formed by n^+ implanting the p-substrate. This implant is relatively shallow and the n^+ layer thickness usually ranges from 0.15 to 0.25 μm. The doping concentration of the n^+ layer is high, usually ranging from 10^{18} to 10^{19} cm^{-3}, while the doping concentration of the p-substrate is low, usually ranging from 10^{15} to 10^{16} cm^{-3}. A layer of gate oxide covers the PD area. Areas covered by field oxide provide pixel-to-pixel (and transistor-to-transistor) electrical isolation. Since the gate oxide is more critical than the field oxide, it is grown at a slower rate such that its quality is high. The gate oxide is thin (about 7 nm in our case) while the field oxide is thick, usually ranging from 0.25 to 0.40 μm. The transition area from the thin gate oxide to the thick field oxide, commonly referred to as "Bird's Beak" (illustrated in Fig. 11), is under enhanced stress. Its interface with the silicon may have a high density of dangling bonds and traps. This transition region is believed to play a significant role in the generation of the pixel dark current in the absence of any radiation. The PD is reverse-biased, with a depletion region width (illustrated in Fig. 11) that usually ranges from 1 to 2 μm, depending on the value of the reverse bias voltage.

The ionizing radiation effects on this pixel structure are very likely to be the buildup (trapping) of positive charge (holes) within the oxide and the creation of interface (silicon/silicon dioxide) states (traps) [20], [28]–[31]. The gate oxide of the devices under consideration is particularly thin; consequently, the effect of holes trapping within the gate oxide is considerably small [20]. The created interface traps that have energy levels within the silicon bandgap contribute to the processes of charge carriers (electrons/holes), emission (generation), and capture (recombination), which leads to an increase in the pixel dark current [29]. The rate of charge carrier recombination R (per unit volume per unit time) can be expressed according to

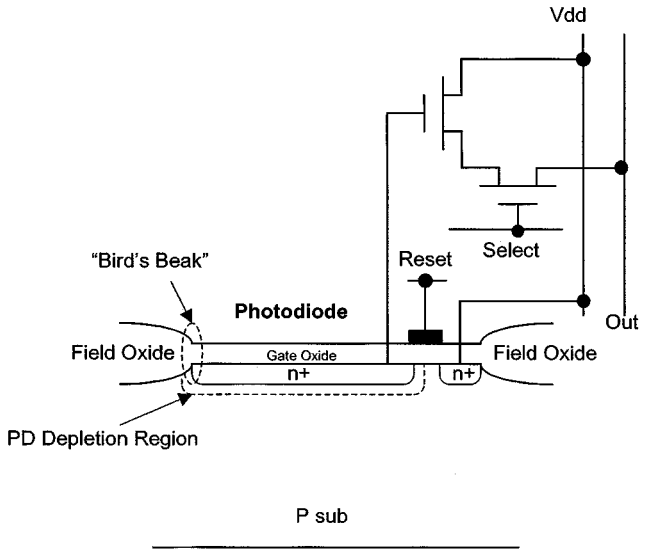

Fig. 11. Schematic illustration of a simplified cross-section of a typical CMOS APS PD pixel (not to scale).

the Shockley–Hall–Read (SHR) theory by the following equation [32]:

$$R = \frac{\sigma_p \sigma_n v_{\rm th} \left(pn - n_i^2\right) N_t}{\sigma_n \left[n + n_i e^{(\frac{E_t - E_i}{kT})}\right] + \sigma_p \left[p + n_i e^{-(\frac{E_t - E_i}{kT})}\right]} \quad (1)$$

where σ_p and σ_n are the hole and electron capture cross-sections, respectively, N_t is the (interface) trap density, E_t is the (interface) trap energy level, E_i is the intrinsic Fermi level, p and n are the hole and electron concentrations, respectively, n_i is the intrinsic carrier concentration, k is Boltzmann's constant, T is the absolute temperature, and $v_{\rm th}$ is the carrier thermal velocity, which is given by the following equation [32]:

$$v_{\rm th} = \sqrt{\frac{3kT}{m^*}} \quad (2)$$

where m^* is the conductivity effective mass.

At thermal equilibrium, $pn = n_i^2$ and the net recombination-generation rate is zero. However, the depletion region of the PD pixel (schematically illustrated in Fig. 11) is depleted from free carriers; thus $n \ll n_i$ and $p \ll n_i$. The depletion region (surface) is in thermal nonequilibrium conditions, and the net generation rate G as a function of the trap energy level E_t may be expressed by the following equation [29]:

$$G(E_t) = -R = \frac{\sigma_p \sigma_n v_{\rm th} n_i N_t}{\sigma_n e^{(\frac{E_t - E_i}{kT})} + \sigma_p e^{-(\frac{E_t - E_i}{kT})}}. \quad (3)$$

This net thermal generation contributes to the pixel dark current. The density of the pixel dark current part that is contributed by the interface traps I_d may be expressed by the following equation [29]:

$$I_d = q \int_0^{E_g} G(E_t)\, dE_t \quad (4)$$

where q is the electronic charge and E_g is the silicon bandgap energy. Equation (4) may be expressed by the following equation [29]:

$$I_d = \left(\frac{\pi}{2} D_t kT \sqrt{\sigma_p \sigma_n}\right) q v_{\rm th} n_i \quad (5)$$

where D_t is the (interface) trap concentration (per unit area per unit energy). To transfer from (4) to (5), D_t was assumed to be uniform across the silicon bandgap. The intrinsic carrier concentration n_i is temperature dependent according to the following proportionality [32]:

$$n_i \propto T^{\frac{3}{2}} e^{-(\frac{E_g}{2kT})}. \quad (6)$$

The dark current density described by (5) is a strong function of the absolute temperature T. Not only does T explicitly appear in (5) but $v_{\rm th}$ is a function of T, as described by (2), and n_i is also a function of T, as described by (6). Furthermore, both the bandgap energy E_g and the intrinsic Fermi level E_i are temperature dependent [32]. An activation energy for dark current generation E_a may be defined such that (5) may be expressed by the following empirical equation [21], [29]:

$$I_d = I_{d\infty} e^{-(\frac{E_a}{kT})} \quad (7)$$

where $I_{d\infty}$ is a constant denoting the mathematical limit of I_d when T approaches ∞. According to (7), the graphical relationship between $\log_e(I_d)$ and $(kT)^{-1}$ is a straight line, and the magnitude of its negative slope is the activation energy E_a.

Previously obtained experimental data of ionizing radiation-induced dark current as a function of temperature validate the analysis presented in this section [21], [22], [28], [33], [34]. These data cover both CMOS APS [21], [22], [28] and CCD [33], [34] image sensors. The activation energy E_a was found to be 0.63 eV in [21], from 0.50 to 0.70 eV in [22], 0.50 eV in [28], 0.63 eV in [33], and 0.50 and 0.68 eV in [34].

The activation energy is highly dependent on the fabrication process but is generally half the bandgap energy E_g, which is 1.12 eV at room temperature [32]. The reason behind this is that the net thermal generation rate $G(E_t)$, expressed by (3), has an acute maximum for the mid-bandgap energy level (at $E_t = E_i$). Interface trap states have a range of energy levels; however, only those levels that are close to mid-bandgap significantly contribute to the net thermal generation and consequently to the dark current.

V. Discussion

The main goal of this research effort is to assess whether CMOS APS image sensors fabricated in standard CMOS fabrication processes can be radiation tolerant. The first step of this assessment process is tolerance to ionizing radiation, which is the subject of this paper. Assessing tolerance to ionizing radiation was selected as a starting point in the assessment process because it is believed that total dose ionizing radiation effects are likely to take place first. Assessments of tolerance to displacement damage and to single event effects are planned for future work but are not the subject of this paper. No claims are

made in this paper regarding the tolerance of CMOS APS image sensors to displacement damage or single event effects.

Utilizing the physical design techniques of enclosed geometry and P-channel guard rings comes with a silicon area penalty. We estimate this silicon area penalty to be increasing the area required by a given pixel by a factor of roughly two. Other work found this penalty factor to range from 1.5 to 3.5, depending on the particular circuit [17]. On the other hand, since an essential ingredient of our approach is the utilization of thin gate oxides, the devices are fabricated in modern standard CMOS fabrication processes. In this research effort, the devices were fabricated in a standard 0.35-μm process that has a gate-oxide thickness of approximately 7.0 nm. Fabricating the devices in modern standard CMOS fabrication processes mitigates the silicon area penalty. This is compared to specialized radiation-tolerant fabrication processes that are usually lagging behind modern fabrication processes by at least one generation. Furthermore, specialized radiation-tolerant processes are more costly by at least a factor of two than modern standard fabrication processes. A comparison was made between the silicon area needed for a set of digital cells designed in a 0.25-μm process using the above-described physical design techniques and that needed for the same cells designed in a 0.60-μm process without using any of those physical design techniques [17]. It was found that the former achieves a higher density, up to a benefit factor of 3.2, depending on the particular cell under consideration. It was further observed that increasing the complexity of the circuit decreases the benefit factor, but in a complete digital circuit it was at least 1.5 [17].

A major concern of this research effort was the dark current performance of the image sensors after having been exposed to high levels of total ionizing radiation dose. Depending on the application, an unacceptably high level of dark current is to deem the image sensor unusable even if it is still functional after having been exposed to high levels of total ionizing radiation dose. The data presented in Fig. 4 show that the increase of dark current with total ionizing radiation dose is rather linear. The rate by which the dark current density increases ranges from about 1 to 2 pA/cm^2/Krd (Si), depending on the pixel design. Table VI shows the dark signal at video rate (30 fps) as a percentage of the saturation signal for each of the four pixels before irradiation, after 1 Mrd (Si) total dose, and after 30 Mrd (Si) total dose. For Pixel0 and Pixel2 at 30 Mrd (Si), the video-rate dark signal is less than 10% of the saturation signal. Pixel1 and Pixel3 are not very far behind, with a video-rate dark signal of about 13% of the saturation signal. This means that for Pixel0 and Pixel2, more than 90% of the pixel signal capacity is available for signal generated by incident photons (as opposed to dark signal), which is considered acceptable for many applications. This performance improves (scales linearly) for applications requiring frame rates higher than 30 fps and degrades for applications requiring frame rates lower than 30 fps. In all applications, independent of the frame rate, this performance is very likely to considerably improve by cooling the image sensor chip. This is because the ionizing radiation-induced dark current is very likely to be an exponential function of temperature as described by (7) in the previous section. Because of logistic reasons, we have not yet performed dark current measurements at temperatures other than room temperature, but these measurements are planned for future work. On the other hand, based on a body of published work [21], [22], [28], [33], [34], and on the analysis presented in the previous section, we believe that the dark current of our devices is very likely to exhibit the same exponential temperature dependence. According to (7), and for an activation energy of 0.6 eV, the dark current performance improvement is about an order of magnitude from room temperature (27 °C) to 0 °C, and about two orders of magnitude from room temperature to −23 °C. The dark current performance improves more with the increase of the activation energy. Lastly, it should be noted that the dark signal as a percentage of saturation signal at 1 Mrd (Si) total ionizing radiation dose is better than that at 30 Mrd (Si) by a factor that ranges from 2.5 to 6.5, depending on the pixel design.

TABLE VI
DARK SIGNAL AT VIDEO RATE (30 FPS) AS A PERCENTAGE OF SATURATION SIGNAL FOR EACH OF THE FOUR PIXELS AT PRERADIATION, AFTER 1 Mrd (SI) TOTAL DOSE, AND AFTER 30 Mrd (SI) TOTAL DOSE

Pixel	Pre-radiation	1 Mrd (Si)	30 Mrd (Si)
Pixel0	0.25%	3.61%	8.79%
Pixel1	0.33%	3.31%	13.21%
Pixel2	0.12%	1.48%	9.61%
Pixel3	0.33%	3.33%	13.07%

The data presented in Fig. 5 show that the responsivity of the image sensors was more or less unchanged after having been exposed to high levels of total ionizing radiation dose. In fact, Pixel2 showed some increase in responsivity from preradiation to a total ionizing radiation dose level of 30 Mrd (Si). The responsivity of an image sensor is a rather complex performance parameter. It quantifies the efficiency by which incident photons are converted to voltage. Responsivity encompasses two major image sensor performance parameters. The first one is quantum efficiency, which quantifies the conversion of incident photons to electrons. Quantum efficiency is dependent on the wavelength of incident photons. The second one is conversion gain, which quantifies the conversion of electrons to voltage. Gaining insight on the behavior of responsivity as a function of total ionizing radiation dose level requires data on quantum efficiency and conversion gain as functions of total ionizing radiation dose level. Measuring quantum efficiency and conversion gain is a very tedious and time-consuming process that could not be performed after each total ionizing radiation dose level within the relatively short time permitted under the MIL-STD-883E, Method 1019.5, Ionizing Radiation (Total Dose) test standard that was followed. Even though the measurement techniques that we adopted were automated, a need for even more automated measurement techniques (such that quantum efficiency and conversion gain can be measured under the above-mentioned standard) does exist. The measurement of quantum efficiency and conversion gain as functions of total ionizing radiation dose level is being considered for future work.

The dark lux data presented in Fig. 6 combine both the responsivity and the dark signal of the image sensor. It is obtained by dividing the dark signal by the responsivity and is rather linear as a function of total ionizing radiation dose level. The dark lux reveals how much equivalent light the image sensor requires to output a voltage signal equal to its dark signal, independent of integration time. The lower the dark lux is for an image sensor, the better its combined dark signal and responsivity performance is. The ratio of the dark lux to the pixel *saturation lux* is the same as the ratio of the dark signal to the pixel saturation signal. Saturation lux is defined as the illumination level in lux that causes the pixel to saturate at a given frame rate. This ratio (dark to saturation) is shown in Table VI for a frame rate of 30 fps (video rate). The dark lux has the same temperature dependence as that of the dark current. Based on a body of published work [21], [22], [28], [33], [34] and on the analysis presented in the previous section, it is very likely that the dark lux performance exhibits the same exponential temperature dependence described by (7), and thus considerably improves by cooling the image sensor chip.

The changes in responsivity, depicted in Fig. 5, may be due to changes in conversion gain and/or changes in quantum efficiency. However, the dark current, depicted in Fig. 4, and the dark lux, depicted in Fig. 6, are rather linear. This leads us to surmise that the conversion gain has remained rather constant as a function of the total ionizing radiation dose. This conjecture is based on the fact that dark signal does not depend on quantum efficiency, as the source of dark signal is not the conversion of incident photons to electrons, which is the fundamental nature of quantum efficiency. The dark signal, however, depends on the conversion gain, which quantifies the conversion of generated electrons (in this case in the absence of incident photons) to voltage. Based on this conjecture, we further surmise that the changes in responsivity are mainly due to changes in quantum efficiency as a function of the total ionizing radiation dose. We do not currently have quantum efficiency or conversion gain data as a function of total ionizing radiation dose to support this conjecture. However, obtaining such data is being considered for future work, as described above.

The design of Pixel1 is almost identical to that of Pixel3. The only difference is that the PD metal contact of Pixel3 is salicided while that of Pixel1 is not. The dark current, responsivity, and dark lux data show that Pixel1 and Pixel3 have nearly identical performances. This suggests that the design difference between the two pixels has minimal effect on their performances. The PD metal contact area is very small compared to either the PD area or the pixel area, and thus the minimal effect of this design difference on the performance was within expectations. Pixel2 has a design feature that distinguishes it from the other three pixels. Each of the other three pixels has a recessed n^+ implant while Pixel2 does not. This design difference was not expected to make a big difference in the responsivity performance. However, the responsivity of Pixel2 is distinct from that of the other three pixels, as it has a fairly low preradiation value, and then shows a noticeable increase as a function of total ionizing radiation dose over the range from 1 to 10 Mrd (Si). As presented above, we surmise that this increase in responsivity is mainly due to increase in quantum efficiency. The recessed n^+ implant is schematically illustrated in Fig. 12, while the nonrecessed n^+ implant is schematically illustrated in Fig. 13. We surmise that the increase in quantum efficiency is due to expansion in the depletion region, particularly near the "Bird's Beak" area. This would lead to more incident photons being absorbed (and hence more electrons being generated) within the depletion region. We further surmise that the additional photons being absorbed would have relatively long wavelengths, i.e., in the red and near infrared region of the frequency spectrum (wavelengths from about 0.6 to about 1.0 μm).

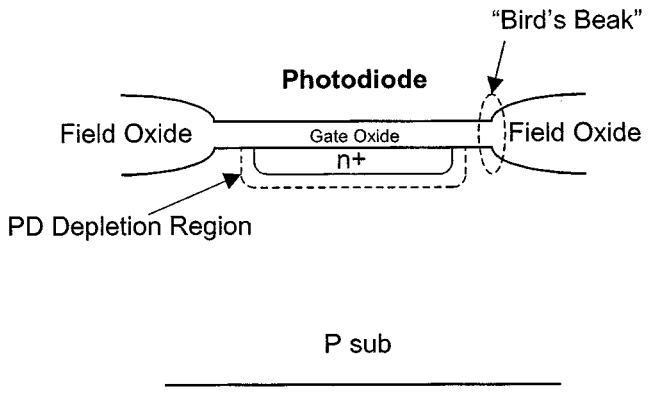

Fig. 12. Schematic illustration of the recessed n^+ implant (not to scale).

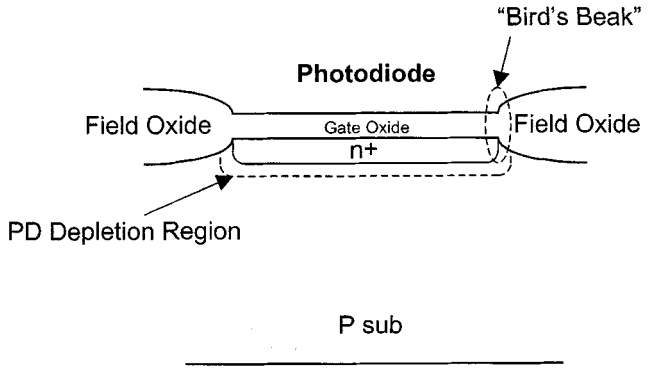

Fig. 13. Schematic illustration of the nonrecessed n^+ implant (not to scale).

Another noteworthy concern of this research effort was the spatial nonuniformity of dark current. The histograms presented in Figs. 7–10 have rather tight distributions. They reveal that the dark current spatial nonuniformity is not as major a concern as was first thought. The worst case dark current spatial nonuniformity is estimated to be about 3–4% of saturation level. This worst case scenario is for a total ionizing radiation dose level of 30 Mrd (Si).

The size of each of the four pixel subarrays is 128×128. Only pixels within an 80×80 window in the center of the subarray were considered for data collection and analysis. This was decided upon for two reasons. The first one is to avoid the edge effect. Pixels of columns and rows near the edges of an image sensor array are in close proximity to the peripheral circuits. Unlike the pixels, peripheral circuits usually have more metal, in terms of both area and number of layers. Also, there is a discontinuity in the layers underneath, as the cross-section of the pixel structure is different from that of the peripheral circuits. Similarly, there is also a discontinuity at the edges

of the four subarrays. The discontinuity and the high density of metal mechanically and electrically stress the pixels of the rows and columns near the edge. Consequently, the dark and optical properties of these pixels are different, and are not a "true" representation of the pixel array. Usually the data from a few edge rows and columns are discarded. For example, if a 1024×1024 image sensor array is required, then it may be designed as 1040×1040, bearing in mind that data from eight lines from each side will be discarded. For the image sensor that is the subject of this paper, perhaps a 120×120 window in the center of the subarray would have been sufficient to avoid the edge effect. However, there is a second reason that necessitated that we trim this window down to 80×80: the practical management of the data collection, storage, and manipulation. For each total dose level, data had to be collected for different values of integration time. For each integration time, data from many frames had to be collected. This was repeated for each pixel type within a chip and for each condition under which the measurements were made. The different conditions ranged from dark to very bright illumination. A number of chips were considered as well. All these measurements had to be performed within the time limit dictated by the above-referenced standard that was followed. We conducted some experimental data analysis, and based on the results of these trials, we chose a set of parameters for the test plan. Our choices of these parameters were such that the data collected have a manageable size that undoubtedly leads to valid results.

The process used to fabricate the devices was a standard 0.35-μm CMOS process. We believe that this fabrication process has two critical factors that significantly contributed to the results. The first factor is the thin gate oxide (about 7 nm in this case), which considerably mitigates the effects of the charge trapped within the oxide [20]. The second factor is that the process was qualified for image sensing technology. This was achieved by designing, fabricating, and characterizing a wide range of test pixels and image sensors (not the subject of this paper). The qualification of the process was based on the results obtained in that phase (no radiation experiments were performed then). It is believed that the fabrication process provides a good starting point (preradiation) in terms of the dark current performance. We surmise that the high preradiation dark current (30 nA/cm^2) reported in [27] is because the process used is not qualified for image sensing technology even though it is qualified as a specialized radiation hard process.

Future planned work includes characterizing the annealing effect on ionizing radiation-induced dark current. Some preliminary measurements were performed nearly two months after irradiation, during which devices were stored unbiased at room temperature. We have observed either no change or a small increase in dark current. The no annealing and/or reverse annealing effects have also been observed in previous work [28], [29], [34], [35]. Future planned work also includes characterizing the ionizing radiation-induced dark current at low temperatures, including obtaining the value of the activation energy. It also includes the measurement of quantum efficiency and conversion gain as functions of total ionizing radiation dose level. Future planned work also includes irradiating the devices by protons and heavy ions to assess the level of their tolerance to displacement damage and to single event effects, including latchup. A next-generation design is currently planned, including the monolithic integration of a radiation-tolerant analog-to-digital converter with the image sensor.

VI. Conclusion

We have demonstrated that CMOS APS image sensors can be designed to be ionizing radiation tolerant to total dose levels up to 30 Mrd (Si). The most pronounced effect on the performance was the increase of dark current, which was linear with total dose level. The rate of dark current increase was about 1 to 2 pA/cm^2/Krd (Si), depending on the design of the pixel. The fabrication process is standard CMOS, yielding a significant cost advantage over specialized radiation hard processes. In addition to their high level of tolerance to ionizing radiation, CMOS APS image sensors have the advantage of being low power. Furthermore, other radiation-tolerant electronics can be monolithically integrated with the CMOS APS image sensor utilizing the same physical design techniques and the same standard CMOS fabrication process, thus enabling miniaturization of radiation-tolerant imaging systems. This combined set of benefits makes CMOS APS technology a viable alternative to CCD technology for many applications in radiation harsh environments such as space applications.

Acknowledgment

The authors would like to thank W. Snoeys of the European Center for Nuclear Research for fruitful discussions in the early stage of this work. The authors would like to acknowledge contributions by their colleagues at Photobit Technology Corporation, Photobit Corporation, the European Center for Nuclear Research, NASA Goddard Space Flight Center, Science Applications International Corporation, and Sandia National Laboratory.

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